Letters

A Control Method for Bridgeless Cuk/Sepic PFC Rectifier to Achieve Power Decoupling

Yonglu Liu, Yao Sun, and Mei Su

***Abstract*—Bulky electrolytic capacitor is usually needed in bridgeless power factor correction rectifiers to buffer the double-frequency ripple power (DFRP). However, it reduces the system reliability and power density significantly. This letter proposed a control method to divert DFRP to the small energy transfer capacitor. Then, the bulky electrolytic capacitor can be replaced with a small film capacitor. The proposed method is realized by making the best of the existing switching states. Therefore, it needs no extra switches or energy storage components, which are usually required in other active power decoupling methods. The operating principle is explained, and a closed-loop control strategy is proposed. Finally, the effectiveness is verified by experimental results.**

***Index Terms*—Active power decoupling, bridgeless power factor correction (PFC) rectifiers, closed-loop control, double-frequency ripple power (DFRP).**

I. Introduction

ACTIVE power factor correction (PFC) circuits are widely employed in rectifiers and switched-mode power supplies to achieve high conversion efficiency and meet harmonic standards like IEC 61000-3-2 [1]. Most PFC circuits comprise a front-end bridge diode rectifier, followed by a basic dc/dc circuit, such as buck, boost, Cuk, Sepic, and Zeta circuit [2], [3]. Consequently, the conduction losses increase because the current path involves three power semiconductors (two diodes in the rectifier and one semiconductor in the dc/dc circuit).

To mitigate the issue, bridgeless PFC circuit topologies have attracted great interests of industry and academy [4]–[11]. In [4]–[6], bridgeless PFC buck and boost rectifiers are proposed by combining the full-bridge diode rectifier with buck and boost circuits. As the usage of semiconductor devices and the number of components in the current path are reduced, the system conversion efficiency is improved, especially under light loads [5]. For wider applications, bridgeless PFC rectifiers based on buck–boost [7], Cuk [8], [9], and Sepic circuit [9]–[11] are proposed.

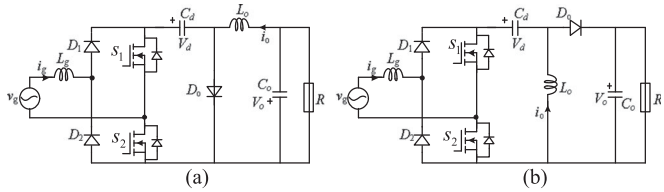

Fig. 1. Bridgeless PFC rectifier based on (a) Cuk [8] and (b) Sepic circuits [10].

Despite the mentioned advantages, a common problem with bridgeless PFC circuit topologies is that a bulky electrolytic output capacitor has to be used to buffer the double-frequency ripple power (DFRP) in the single-phase system [12], [13]. However, it is well known that electrolytic capacitors are the most vulnerable links and more than half of faults are caused by degraded electrolytic capacitors [14]–[16]. Moreover, the size is enlarged with the use of the bulky electrolytic capacitors.

To improve the reliability and power density of the bridgeless Cuk/Sepic PFC rectifier, a new control method is proposed to decouple the ripple power. The idea behind the proposed control is to use the existing energy transfer capacitor in Cuk/Sepic converter to buffer the DFRP. Then, the large output capacitor can be replaced with a small film capacitor. Experimental results verify the effectiveness of the proposed method.

II. Bridgeless PFC Rectifiers

Fig. 1 shows the proposed bridgeless Cuk and Sepic PFC rectifiers in [8] and [10]. They are obtained by combining a Cuk/Sepic dc/dc circuit with a full-bridge diode rectifier. In [8] and [10] the research is focused on the circuit structure, and the operation principles follow the conventional Cuk/Sepic PFC rectifier. With that operating mode regime switches S_1 and S_2 are synchronously turned ON and OFF (named the conventional control method). When S_1 and S_2 are both turned OFF, the power is transferred to energy transfer capacitor C_d. When S_1 and S_2 are both turned ON, the power (including DFRP) stored in C_d is fully transferred to the load side. Then, a bulky electrolytic

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The authors are with the School of Information Science and Engineering, Central South University, Changsha 410083, China (e-mail: liuyonglu@csu.edu.cn; yaosuncsu@gmail.com; sumeicsu@mail.csu.edu.cn).

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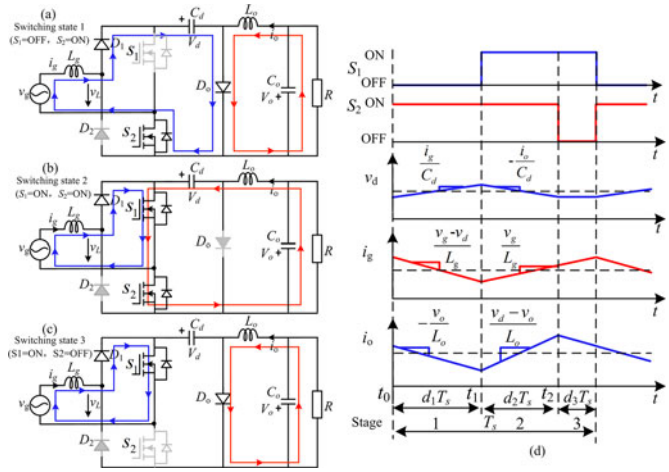

Fig. 2. Switching states of bridgeless Cuk PFC rectifier in the positive half-line cycle and theoretical waveforms. (a) State 1. (b) State 2. (c) State 3. (d) Theoretical waveforms.

capacitor C_o has to be employed to buffer the DFRP and, hence, smooth the output voltage.

III. Proposed Control Method

A. Operation Principle

Due to the symmetrical operation in two half-line cycles of the grid voltage, the operation principle is explained only in the positive half-line cycle. It is assumed that the rectifier operates under the continuous conduction mode, input voltage is pure sinusoidal, all the components are ideal and lossless, and the switching voltage ripples are negligible during the switching period T_s. In this section, the bridgeless Cuk PFC rectifier is taken as an example to explain the proposed control method in detail. Three used switching states of bridgeless Cuk rectifier are shown in Fig. 2(a), (b), and (c).

The whole operation process is divided into three distinct operating stages, as shown in Fig. 2(d). d_i $(i = 1, 2, 3)$ is the duty ratio of the switching state i. The operating stages over a switching cycle are briefly described as follows.

Stage 1[t_0, t_1], [see Fig. 1(a)]: In this stage switch S_1 is turned OFF and switch S_2 is turned ON. The currents i_g and i_o are decreased and the voltage v_d is increased.

Stage 2[t_1, t_2], [see Fig. 1(b)]: In this stage both switches S_1 and S_2 are turned ON. The currents i_g and i_o are increased and the voltage v_d is decreased.

Stage 3[t_2, T_s], [see Fig. 1(c)]: In this stage switch S_1 is turned ON and switch S_2 is turned OFF. The current i_g is increased, current i_o is decreased, and the voltage v_d remains. This stage is used to prevent the DFRP from flowing into the load. However, in the conventional control method [8] this stage is not used.

The state-space average model is formulated as follows:

$$L_g \frac{di_g}{dt} = v_g - d_1 v_d \tag{1}$$

$$C_d \frac{dv_d}{dt} = d_1 i_g - d_2 i_o \tag{2}$$

$$L_o \frac{di_o}{dt} = d_2 v_d - v_o \tag{3}$$

$$C_o \frac{dv_o}{dt} = i_o - \frac{v_o}{R_o} \tag{4}$$

where $d_1 + d_2 \leq 1$.

In the conventional control method, there are only two switching states: S_1 and S_2 are both turned OFF [equivalent to switching state 1 in Fig. 1(a)] and turned ON [equivalent to switching state 2 in Fig. 1(b)]. And its state-space average model can also be expressed by (1)–(4). The only difference is the sum of d_1 and d_2 is 1 due to the absence of switching state 3. Consequently, there is only one degree of freedom. It is difficult to guarantee the performance of the input current and the output voltage simultaneously. However, in the proposed control method, the constraint of the sum of d_1 and d_2 is not more than 1. Therefore, there are two degrees of freedom and both the input current and the output voltage can be controlled independently.

B. Steady-State Analysis

The current i_g is supposed to be

$$i_g = I\cos(\omega t) \tag{5}$$

where I is the amplitude of the grid current and ω is the angular frequency of the grid voltage. Then, according to (1) and (5), we have

$$\begin{cases} L_g \dfrac{di_g}{dt} = v_g - v_L = -\omega I L_g \sin(\omega t) \\ v_L = d_1 v_d. \end{cases} \tag{6}$$

From (6), the steady state d_1 can be obtained as

$$d_1 = \frac{v_L}{v_d} = \frac{v_g + \omega I L_g \sin(\omega t)}{v_d}. \tag{7}$$

According to (3), the steady state d_2 is expressed as

$$d_2 = \frac{v_o}{v_d}. \tag{8}$$

Since $\sum d_i = 1$, d_3 is expressed as

$$d_3 = 1 - d_1 - d_2. \tag{9}$$

Suppose that all the DFRP is buffered by the capacitor C_d, then voltage v_d could be expressed as

$$v_d = \sqrt{\bar{v}_d^2 + \frac{VI\sin(2\omega t)}{2\omega C_d}} \tag{10}$$

where $\bar{v}_d$ is the dc component of v_d, and V is the amplitude of the grid voltage. Note that $\bar{v}_d$ is a degree of freedom. With the consideration of the limitation $0 \leq d_i \leq 1$ and the permissible maximum voltage $V_{\max}$ on semiconductors and passive components, the range of $\bar{v}_d$ is expressed as

$$\sqrt{(v_g + v_o + \omega I L_g \sin(\omega t))^2 - \frac{VI\sin(2\omega t)}{2\omega C_d}} \leq \bar{v}_d \leq \sqrt{V_{\max}^2 - \frac{VI\sin(2\omega t)}{2\omega C_d}}. \tag{11}$$

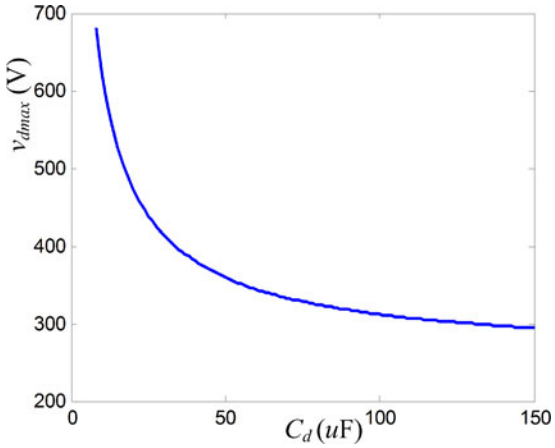

Fig. 3. Plot of voltage stress against the capacitance.

Usually, the voltage drop on the inductor L_g is small and could be ignored. Thus, $\bar{v}_d$ could be chosen as follows:

$$\begin{cases} \sqrt{(V+v_o)^2+\dfrac{VI}{2\omega C_d}} \le \bar{v}_d \le \sqrt{V_{\max}^2-\dfrac{VI}{2\omega C_d}} \\ \sqrt{(V+v_o)^2+\dfrac{VI}{\omega C_d}} \le V_{\max} \end{cases}. \quad (12)$$

Then, the voltage stress of capacitor C_d is

$$v_{d\,\max}=\sqrt{\bar{v}_d^2+\tfrac{VI}{2\omega C_d}}. \quad (13)$$

According to (10) and (12), the minimal voltage stress of C_d is $\sqrt{(V+v_o)^2+VI/(\omega C_d)}$, which is larger than $(V+v_o)$ (voltage stress of C_d in the conventional control method).

With considering $\bar{v}_d$ being its lower limit and the parameters using in this letter, the voltage stress $v_{\max}$ against the capacitor C_d is shown in Fig. 3. Clearly, there is a tradeoff between the capacitance and the voltage stress. Besides, when C_d is increased to be a certain value, increasing C_d would not reduce the voltage stress dramatically. Therefore, a decoupling capacitance of 100 uF is selected in this study.

C. Controller Design

There are two control goals: grid current and output voltage regulations. According to (3) and (4), the output side can be viewed as a buck converter and d_2 can be used to regulate the output voltage. Therefore, many control methods for buck converter can be applied. In this letter, a simple double-loop control strategy is adopted, as shown in Fig. 4. Its output is the averaged voltage reference v_o^*, which is used to calculate d_2 according to (8).

To realize the control objectives, the dc component of the energy transfer capacitor voltage $\bar{v}_d$ is controlled to be a given value [17]. Whereas, the instantaneous value v_d swings at low frequency as a result of buffering the DFRP. The control of $\bar{v}_d$ is achieved by regulating the amplitude reference of the grid current, as shown in Fig. 4. At last, the PFC is realized by controlling the grid current being in phase with the grid voltage. The phase information of grid voltage is obtained by a phase-locked loop. To track the given sinusoidal grid current reference, according to the internal model principle, a proportional resonant (PR) controller is used for the current loop. Its output is the averaged voltage reference v_L^*, which is used to calculate d_1 according to (7).

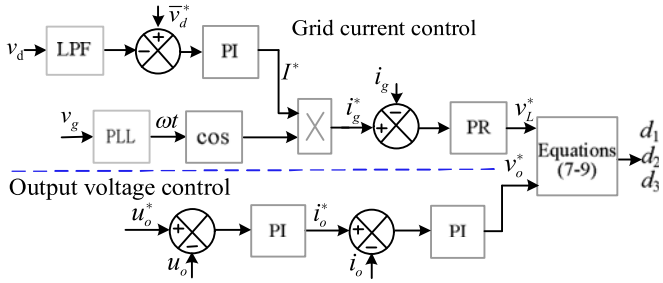

Fig. 4. Block diagram of the control scheme.

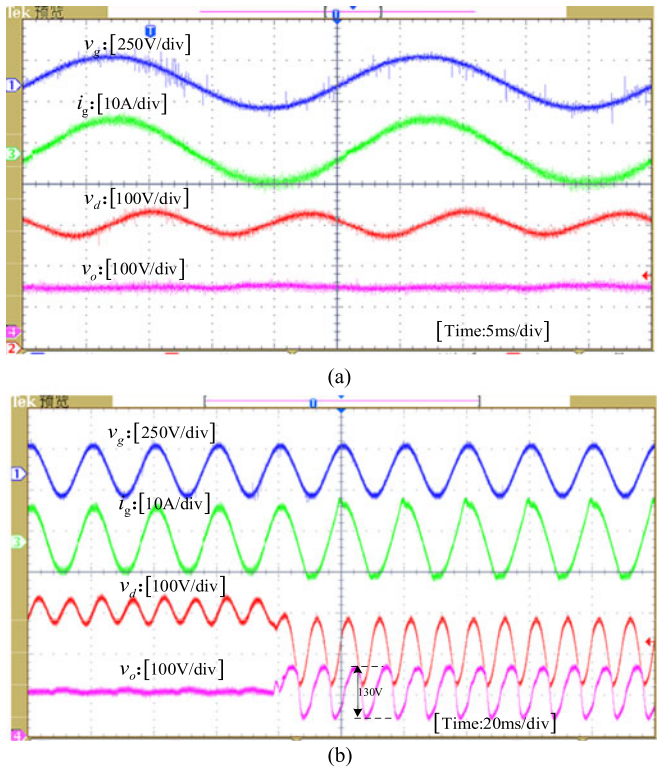

Fig. 5. Experimental waveforms of grid voltage v_g, grid current i_g, capacitor voltage v_d, and load voltage v_o. (a) Steady-state experimental waveforms. (b) Dynamic experimental waveforms.

IV. Experimental Results

To verify the theoretical analysis an experimental prototype of the bridgeless Cuk PFC rectifier was built and tested. It was designed for 110-$V_{\rm rms}$ ac-input, 100-V dc-output, 500-W rated power, and runs at $f_s = 20$ kHz. L_g and L_o are both 3 mH. C_d and C_o are both film capacitors with the values of 100 μF/ 450 V and 10 μF/ 100 V, respectively. The dc component of v_d is set to 310 V. Semiconductors used were IPW60R099P6 MOSFETs and DSEI60-06A diodes. The control algorithm of the converter

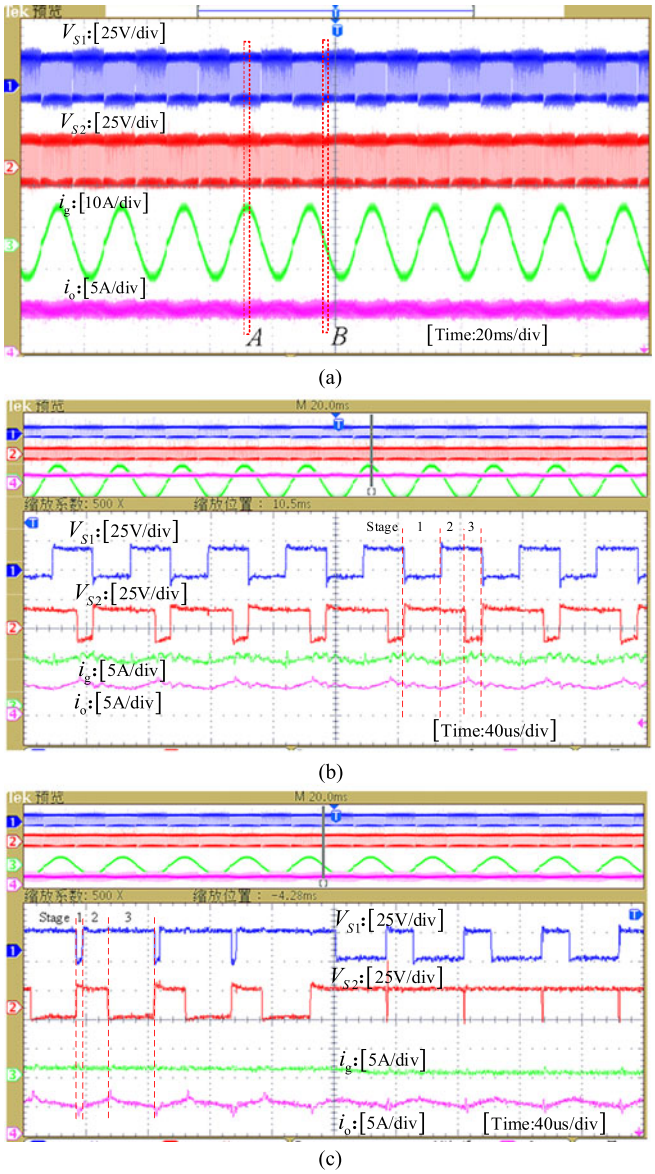

Fig. 6. Experimental waveforms of gate-emitter voltages, grid current i_g, and inductor current i_o. (a) Waveforms of V_{s1}, V_{s2}, i_g, and i_o. (b) Zoom-in waveforms of point *A*. (b) Zoom-in waveforms of point *B*.

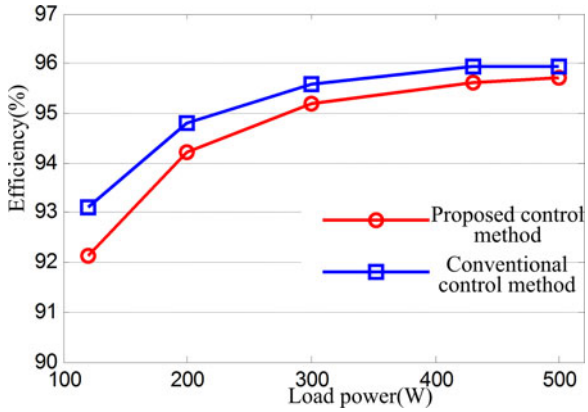

Fig. 7. System efficiency curves.

is realized on a universal control board (digital signal processor TMS320F28335 and FPGA EP2C8T144C8N).

The steady-state experimental waveforms are shown in Fig. 5(a). As seen, the grid current i_g is sine shaped and in phase with the grid voltage v_g. The power factor is 0.99. The output voltage is smooth and the ratio of the second-order harmonic component to the dc component is about 0.78%. To realize the same voltage ripple level with a bulky capacitor, the required capacitance is 7200 μF/ 100 V. Therefore, although the value of C_d is larger than that in the conventional method (a few microfarads), the total volume of the capacitors (evaluated by the product of capacitance and voltage rating [18]) is reduced. In addition, the lifespan is extended greatly. Capacitor voltage v_d swings at double-frequency grid voltage as a result of buffering the ripple power. Fig. 5(b) illustrates the experimental waveforms when the proposed control method is suddenly disabled and the conventional control method works. The DFRP flows into the load side and causes a low-frequency fluctuation of the output voltage. The peak–peak value of output voltage v_o is up to 130 V. The decoupling capacitor voltage returns to following the sum of the output voltage and the rectified grid voltage [8] and also swings at twice the grid voltage frequency. Besides, the grid current is distorted. The experimental results indicate the validity of the proposed control method.

Fig. 6 shows the gate-emitter voltages, grid current i_g, and inductor current i_o. V_{s1} and V_{s2} are the gate-emitter voltages of switches S_1 and S_2. As seen, switches S_1 and S_2 are driven by different drive signals and their patterns are different from each other. But in conventional control method switching S_1 and S_2 are synchronously turned ON and OFF.

Fig. 7 illustrates the efficiency curves with the proposed and conventional control methods. In the conventional control method, C_d is a 2-μF film capacitor and C_o is a 6800-μF electrolytic capacitor. The efficiency with the proposed control method is slightly lower. The main reason is the increased voltage stress of the capacitor C_d as introduced in Section III. That increases the switching losses of switches and diodes [19]. As reported in [20], usually the efficiency penalty is more than two percentage points in active power decoupling methods. However, the system efficiency drop under rated load power is only about 0.4% in the proposed method. This issue can be mitigated by using advanced semiconductor devices, such as SiC or GaN MOSFETs [21].

V. Conclusion

In this letter, a new control method was proposed for bridgeless Cuk/Sepic PFC rectifier to reduce the output filter capacitance. Then, the power density and system reliability were improved. A 500-W laboratory prototype was built to verify the effectiveness. The control method will promote the proliferation of the bridgeless Cuk/Sepic PFC rectifier in volume-critical, weight-critical, and/or lifetime-critical applications. In addition, it requires no any extra hardware and could also be extended to other type of bridgeless PFC rectifier. However, it also has some shortcomings, such as increased control complexity and costs, voltage stress, and power losses. Thus, in the further study, we

will focus on simplifying the control algorithm and developing low-cost control systems, such as specialized chips, low-cost digital control system, or analog digital hybrid control system. On the other hand, multiobjective optimization methods will be studied to select the value of C_d by comprehensively considering voltage stress, efficiency, volume, and costs. Besides, advanced semiconductor devices will be used to improve the efficiency.

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